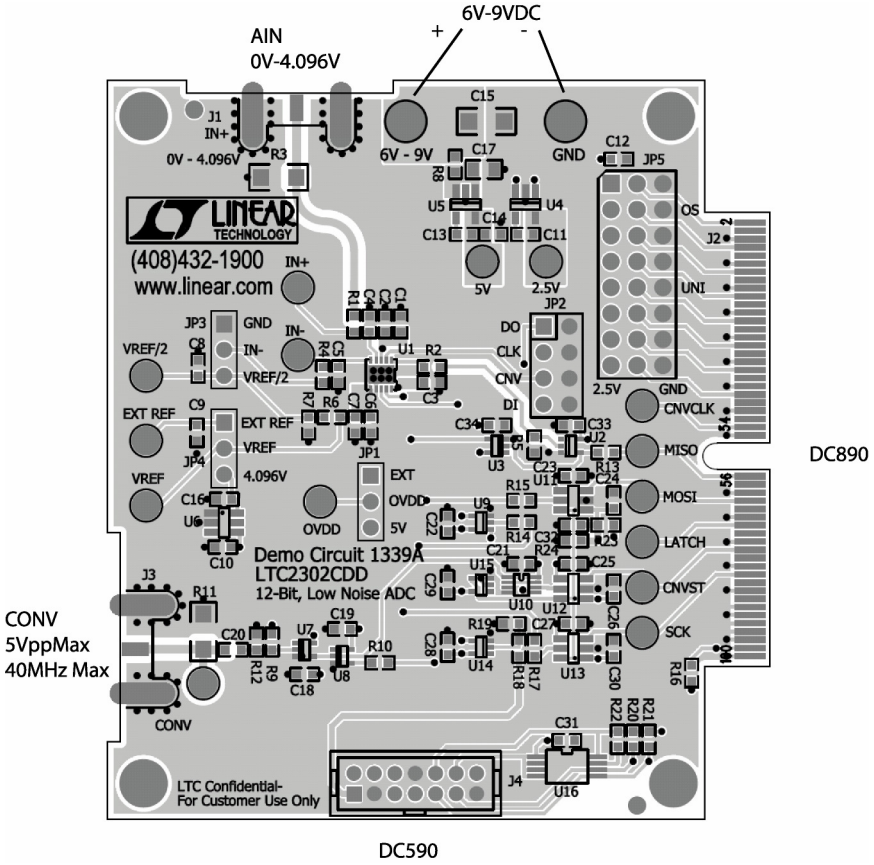
DESCRIPTION

Demonstration circuit 1339 features the LTC2302 low noise, 500ksps, 12-Bit, ADC. The LTC2302 has an SPI compatible serial interface that can be used to select channel polarity and unipolar or bipolar settings. DC1339A demonstrates the DC and AC performance of the LTC2302 in conjunction with the DC590B QuikEval and DC890B Fast DAACS data collection boards. Use DC590B to demonstrate DC performance such as peak-to-peak noise and DC linearity. Use DC890B if precise sampling rates are required or to demonstrate AC performance such as SNR, THD, SINAD and SFDR. Alternatively, by connecting the DC1339A into a customer application, the performance of the LTC2302 can be evaluated directly in that circuit.

Design files for this circuit board are available. Call the LTC factory.

Figure 1. DC1339A Connection Diagram



DC890B QUICK START PROCEDURE

Connect DC1339A to a DC890B USB High Speed Data Collection Board using connector J2. Connect DC890B to a host PC with a standard USB A/B cable. Apply 6V-9V DC to the 6V-9V and GND terminals. Apply a low jitter signal source to IN+ on connector J1. Apply a low jitter clock with a maximum frequency of 40MHz to connector J3. The clock can be a sine wave or square wave with maximum amplitude of 14dBm. Note that J3 has a 50Ω termination resistor to ground, which will prevent most logic from driving this pin directly. Run the Fast DAACS software (Pscope.exe version K51 or later) supplied with DC890B or download it from www.linear.com. Complete software documentation is available from the Help menu. Updates can be downloaded from the Tools menu. Check for updates periodically as new features may be added.

PSCOPE SOFTWARE CONFIGURATION

The Pscope software will recognize DC1339A and configure itself automatically. The default configuration is for IN+ with respect to IN- in unipolar mode. Make sure that the jumpers are set as shown in Figure 2. If bipolar mode is desired, it will be necessary to change the Pscope ADC configuration setting as well as jumpers JP3 and JP5. From the front page of the software select ADC Configuration from the Configure menu. Select 12-Bits, Alignment 12, FPGA Ld Serial 2308 Class, 1-Channel. Do not check Positive Edge Clk. Check Bipolar if the JP5 UNI jumper is set to GND. An example of the ADC configuration menu is shown in Figure 3. JP3 should be changed from GND to VREF/2 in bipolar mode, so that the minus input is biased halfway between ground and Vref.

Click the Collect button (See Figure 4) to begin acquiring data. Depending on which board was previously used by Pscope it may be necessary to press Collect a second time. The Collect button then changes to Pause, which can be used to pause data acquisition.

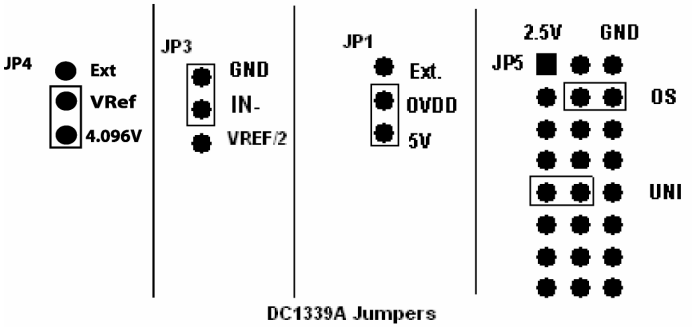


Figure 2. Jumper Settings

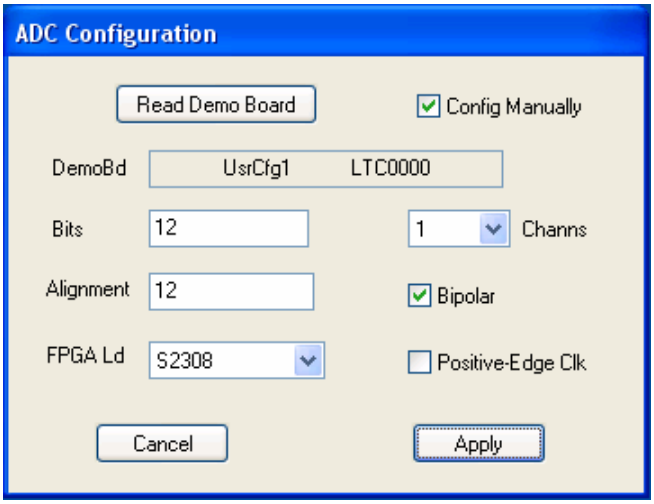


Figure 3. User Configure Menu

DC590B QUICK START PROCEDURE

Connect DC1339A to a DC590 USB serial controller using the supplied 14-conductor ribbon cable. Connect DC590 to a host PC with a standard USB A/B cable. Run the evaluation software supplied with DC590 or download it from www.linear.com. The correct control panel will be loaded automatically. Version K73 of QuikEval or higher should be used for this board. Click the COLLECT button to begin reading the ADC. Change the range (unipolar or bipolar) by right clicking over the range indicator in the display. See Figure 5.

HARDWARE SET UP

SIGNAL CONNECTIONS

J1 SMA connector for IN+. Limit input swings to 0V-4.096V. For optimum performance, the input should be band limited to the frequencies of interest. See schematic for details.

J2 FastDAACS interface to DC890B. Do not use J4 at the same time.

J3 Conversion Clock Input. This input has a 50Ω termination resistor, and is intended to be driven by a 14dBm sine or square wave. To achieve full AC performance of this part, the clock jitter should be kept under 20ps. This input is capacitively coupled to a clock buffer so that level shifting is not required. To run at maximum conversion rate, apply a 40MHz signal to this connector. J3 is used only for DC890B. DC590B generates its own clock signal.

J4 Quick Eval interface to DC590B. Do not use J2 at the same time. This connector can also be used to drive the ADC directly. See schematic for details.

JUMPERS

JP1 (OVDD) connects the OVDD pin of the ADC to 5V or to an external voltage. The SDO pin swings from ground to OVDD.

JP2 contains CONV, SDI, SCK and a buffered SDO signal. This connector is intended to monitor these signals. For for those who want to drive the ADC directly use J4.

JP3 (IN-) selects whether the IN- pin of the ADC is to be cleanly grounded near the ADC or connected to VREF/2.

JP4 (VREF) selects onboard or external reference for the ADC

JP5 (DIN Word) selects the channel configuration and unipolar/bipolar settings of the ADC. (JP5 is used by the DC890B only. It is ignored by the DC590B.)

GROUNDING AND POWER CONNECTION

Connect a 6V to 9V power supply to the 6-9VDC and GND posts when using DC890B. If the DC590B is used it will provide power to the DC1339.

Figure 4. DC1339A Pscope Screenshot

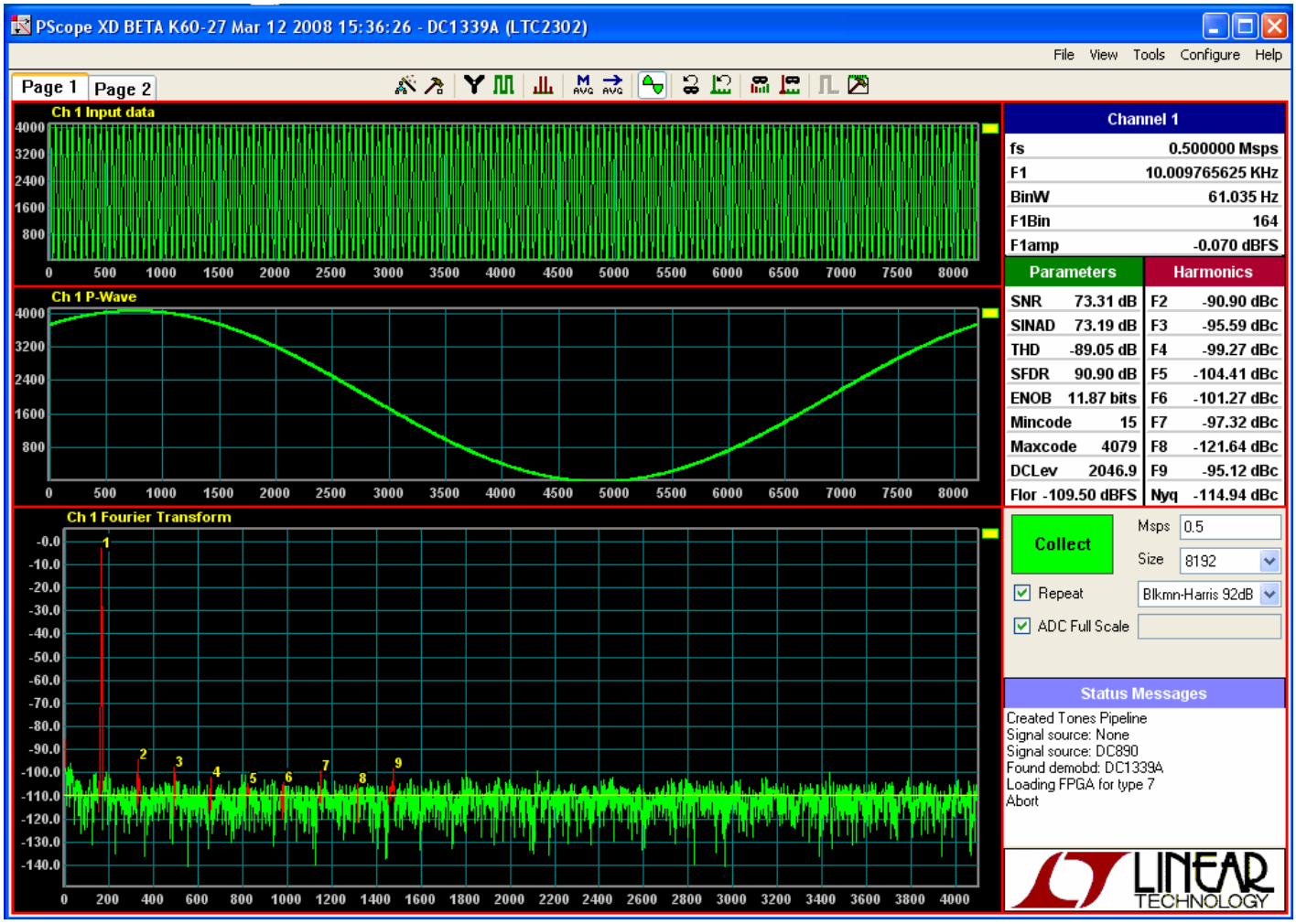
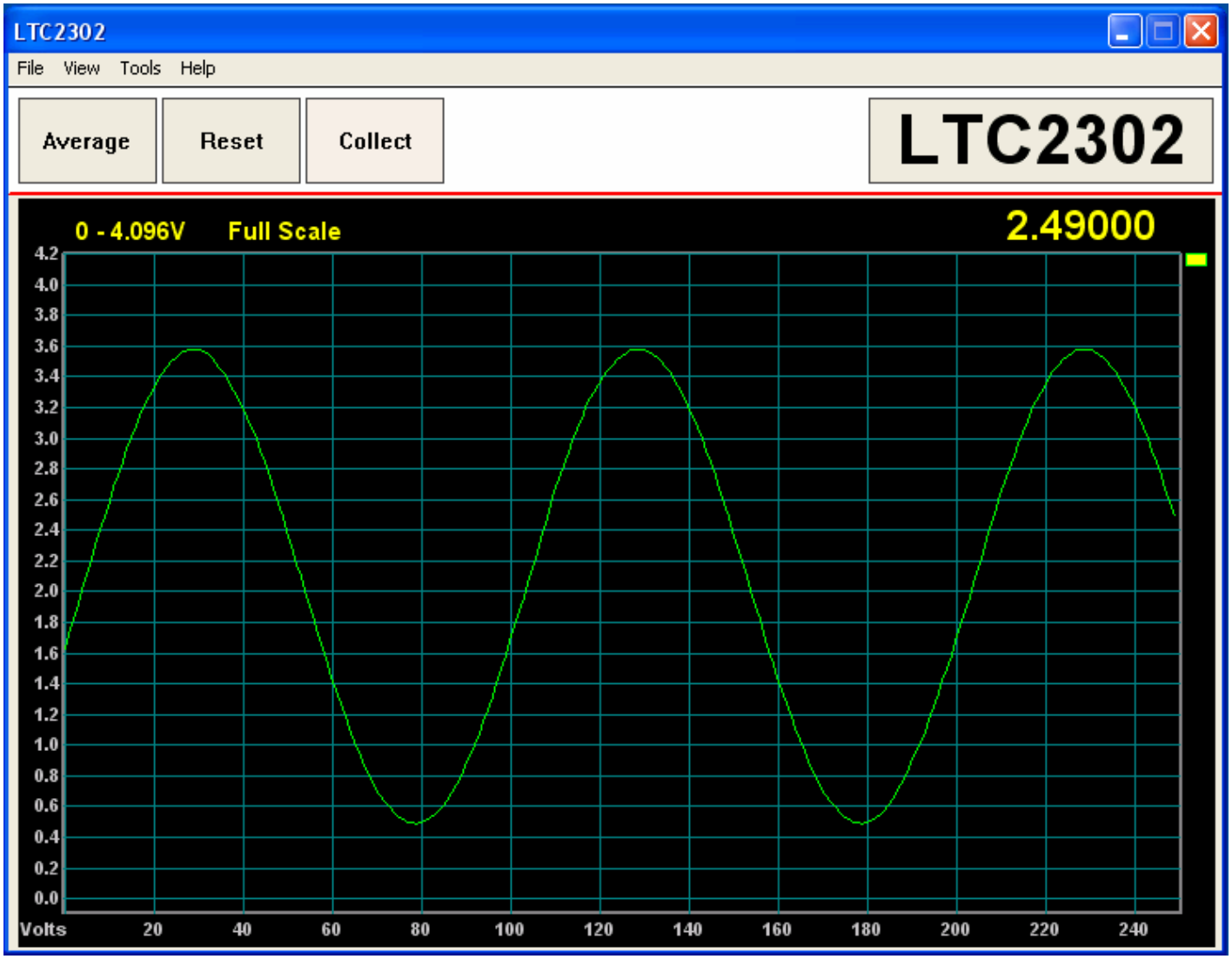
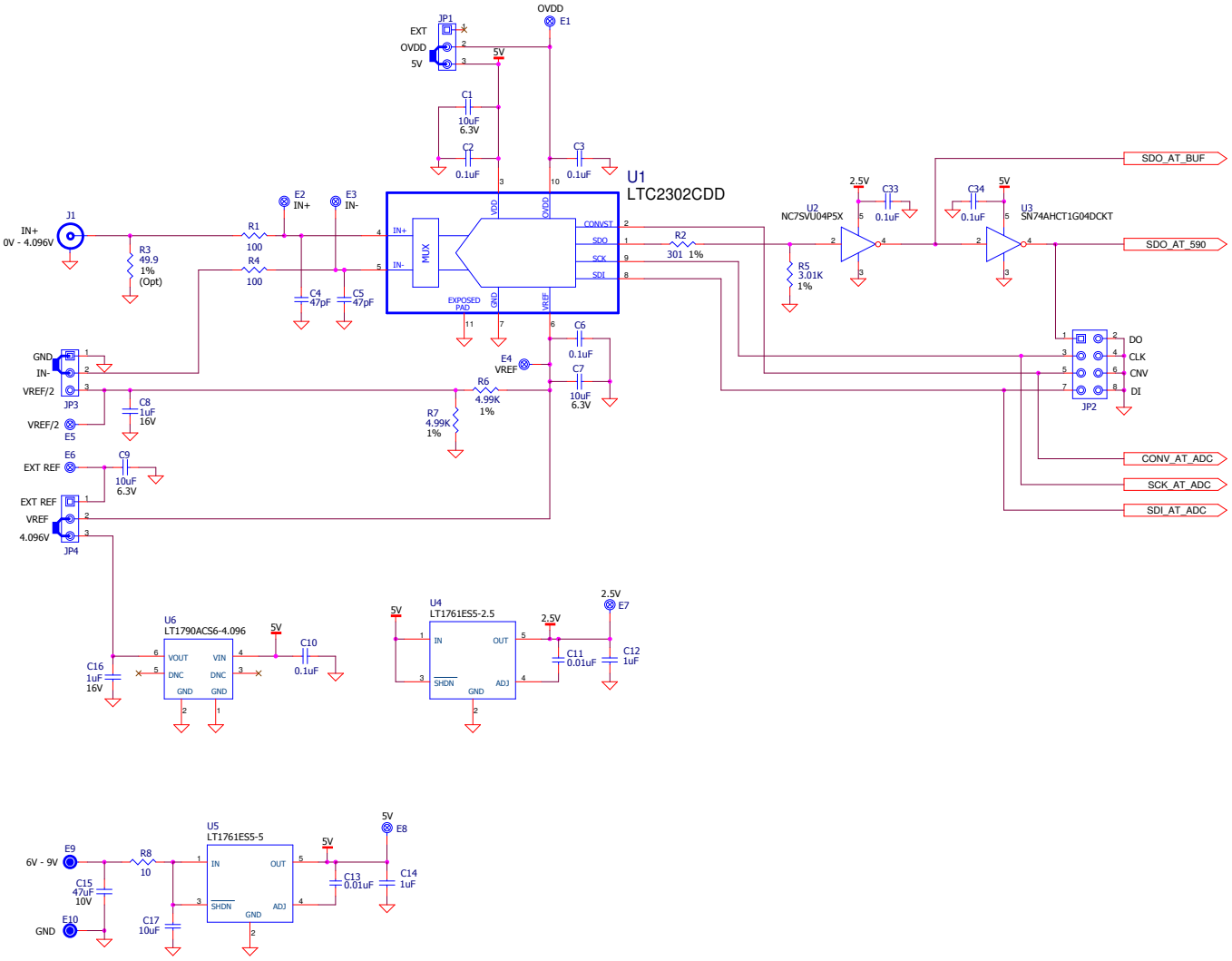
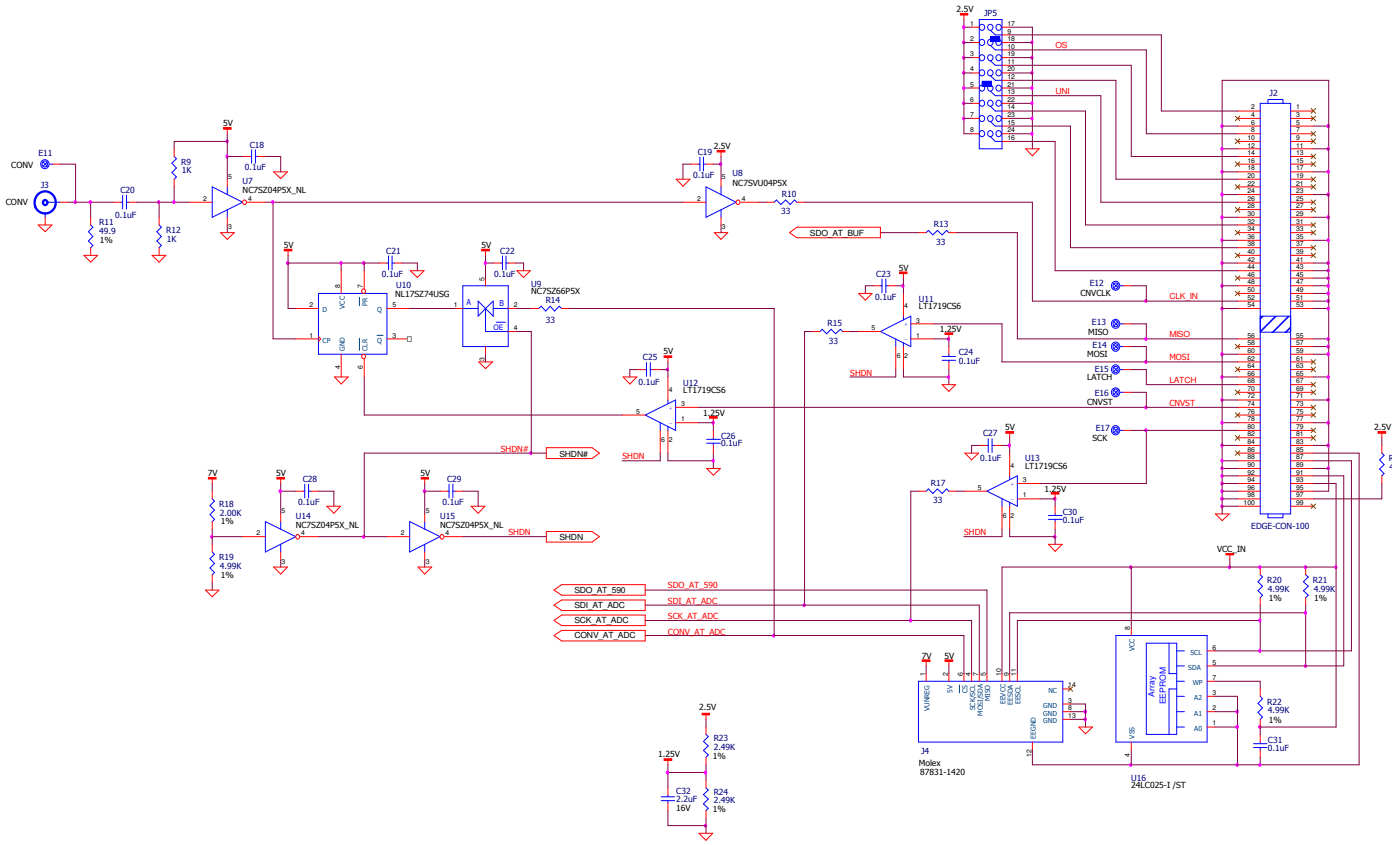


Figure 5. DC1339A QuikEval Screen Shot




U1
LTC2302CDD
U2
NC7SVU04P5X
U3
SN74AHCT1G04DCKT
U4
LT1761ES5-2.5
U5
LT1761ES5-5
U6
LT1790ACS6-4.096
JP1
JP2
JP3
JP4
J1
OVDD
5V
2.5V
IN+
0V - 4.096V
IN-
VREF/2
EXT REF
4.096V
6V - 9V
GND
SDO_AT_BUF
SDO_AT_590
CONV_AT_ADC
SCK_AT_ADC
SDI_AT_ADC
DO
CLK
CNV
DI


JP5
J2
EDGE-CON-100
U7 NC7SZ04P5X_NL
U8 NC7SVU04P5X
U9 NC7SZ66P5X
U10 NL17SZ74USG
U11 LT1719CS6
U12 LT1719CS6
U13 LT1719CS6
U14 NC7SZ04P5X_NL
U15 NC7SZ04P5X_NL
U16 24LC025-I /ST
J4 Molex 87831-1420
CONV
OS
UNI
CLK_IN
MISO
MOSI
LATCH
CNVST
SCK
SDO_AT_BUF
SDO_AT_590
SDI_AT_ADC
SCK_AT_ADC
CONV_AT_ADC
SHDN
SHDN#
VCC_IN
2.5V
5V
7V
1.25V