



MAX3638 Evaluation Kit

General Description

The MAX3638 evaluation kit (EV kit) is a fully assembled and tested demonstration board that simplifies evaluation of the MAX3638 low-jitter, wide-frequency range clock generator. The EV kit includes an on-board 25MHz crystal and switches for selecting different modes of operation. The reference inputs and clock outputs use SMA connectors and are AC-coupled to simplify connection to test equipment.

EV Kit Contents

◆ MAX3638 EV Kit Board

DESIGNATION	QTY	DESCRIPTION
C1–C10, C14, C15, C16, C18–C24, C27–C32, C34–C37	30	0.1 μ F \pm 10% ceramic capacitors (0402)
C11	1	2.2 μ F \pm 10% ceramic capacitor (0603)
C12	1	0.1 μ F \pm 10% ceramic capacitor (0603)
C13	1	33 μ F \pm 10% tantalum capacitor (B case) AVX TAJB336K010R
C17	1	27pF \pm 10% ceramic capacitor (0402)
C25	1	33pF \pm 10% ceramic capacitor (0402)
C26	1	10 μ F \pm 10% ceramic capacitor (0603)
C33	1	3pF \pm 10% ceramic capacitor (0402)
J1–J9, J11, J13–J24	22	SMA connectors, edge-mount, tab contact Johnson 142-0701-851
J10, J12	2	Test points Keystone 5000
L1, L4, L5, L8, L9, L11, L13, L16, L17, L20, L21, L24, L25, L28, L29, L32, L35, L36	18	Ferrite beads (0402) Murata BLM15HD102SN1

Features

- ◆ Fully Assembled and Tested
- ◆ On-Board 25MHz Crystal
- ◆ Switches for Selecting Modes of Operation
- ◆ SMA Connectors and AC-Coupled Clock I/Os

Ordering Information

PART	TYPE
MAX3638EVKIT+	EV Kit

+Denotes lead(Pb)-free and RoHS compliant.

Component List

DESIGNATION	QTY	DESCRIPTION
L2, L3, L6, L7, L10, L12, L14, L15, L18, L19, L22, L23, L26, L27, L30, L31, L33, L34	18	4.7 μ H \pm 10% inductors (0805) Murata LQM21NN4R7K10
R1–R10, R12, R15–R18, R20, R21, R22	18	150 Ω \pm 1% resistors (0402)
R11	1	49.9 Ω \pm 1% resistor (0402)
R13	1	10.5 Ω \pm 1% resistor (0402)
R14	1	33.2 Ω \pm 1% resistor (0402)
R19	1	499 Ω \pm 1% resistor (0402)
S1, S2, S3, S5–S17	16	Switches, SP3T, slide ALPS SSS211900
S18–S21	4	Switches, SPDT, slide E-Switch EG1218
TP1, TP2	2	Test points Keystone 5000
U1	1	Clock generator (48 TQFN-EP*) Microsemi MAX3638ETM+
U2	1	25MHz crystal NDK EXS00A-AT00429
—	1	PCB: MAX3638 EVALUATION BOARD+, REV B

*EP = Exposed pad.

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Quick Start

- Set the switches to the following settings to generate a 125MHz LVDS output from the 25MHz crystal reference:
 - IN_SEL = XO
 - PLL_BP = LOW
 - DM = LOW
 - DP = LOW
 - DF1 = LOW, DF0 = OPEN
 - DA1 = OPEN, DA0 = HIGH
 - DB1 = OPEN, DB0 = HIGH
 - DC1 = HIGH, DC0 = LOW
 - QA_CTRL1 = LVDS
 - QA_CTRL2 = DISABLED
 - QB_CTRL = DISABLED
 - QC_CTRL = DISABLED
 - QA_TERM1 = LVDS
 - QA_TERM2 = LVDS
 - QB_TERM = LVDS
 - QC_TERM = LVDS
- Connect a +3.3V supply to VCC (J10) and GND (J12). Set the supply current limit to 500mA.
- Using SMA cables, connect QA0 (J11) and $\overline{\text{QA0}}$ (J13) to a phase noise analyzer or scope. Terminate all unused enabled outputs, QA1 (J14), $\overline{\text{QA1}}$ (J15), QA2 (J16), and $\overline{\text{QA2}}$ (J17).

Detailed Description

The MAX3638 EV kit simplifies evaluation by providing the hardware needed to evaluate all the MAX3638 functions. Table 1 contains functional descriptions for the switches. Table 2 provides the divider settings for various frequency configurations.

LVC MOS Clock Input

The LVC MOS clock input, CIN, is AC-coupled at the SMA connector and has an on-board 50 Ω termination. For optimal performance it is important to use a low-jitter square-wave clock source. Clock signals should be applied to CIN only when the switch IN_SEL is set to CIN.

Differential Clock Input

The differential clock input, DIN, is AC-coupled at the SMA connectors and has an internal 100 Ω differential termination. For optimal performance it is important to use a low-jitter, differential, square-wave clock source. Clock signals should be applied to DIN only when the switch IN_SEL is set to DIN.

LVDS/LVPECL Clock Outputs

The LVDS/LVPECL clock outputs (QA[4:0], QB[2:0], QC) are configured using switches S14–S21. Each output has an on-board bias-T, which provides DC bias when configured as LVPECL and AC-coupling for direct connection to 50 Ω -terminated test equipment. Unused outputs should be disabled (using switches S14–S17) or have 50 Ω terminations placed on the SMA connectors. For optimal jitter measurements, a balun is recommended for differential to single-ended conversion when connected to single-ended test equipment such as a phase noise analyzer. See Figure 1 for the measurement setup.

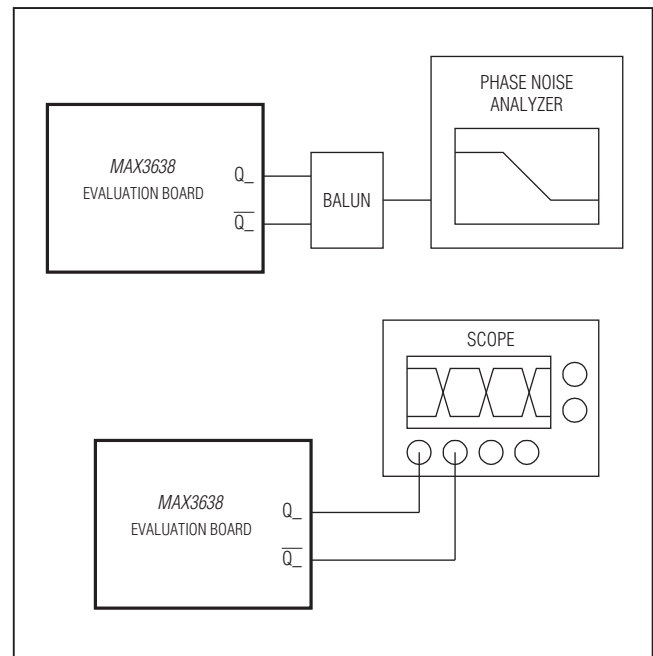


Figure 1. Measurement Setup

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LVC MOS Clock Output

The LVC MOS clock output, QCC, has a 500Ω series load resistor and is AC-coupled at the SMA connector. This output can be connected to 50Ω-terminated test equip-

ment, or a high-Z (1MΩ) scope probe. If connected to 50Ω test equipment, the output swing at the termination is approximately 275mV_{p-p}.

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Table 1. Switch Descriptions

COMPONENT	NAME	FUNCTION
S1	IN_SEL	Selects input reference clock source. DIN = Differential input DIN, $\overline{\text{DIN}}$ CIN = LVC MOS input CIN XO = Crystal reference (25MHz on-board)
S2	PLL_BP	Selects PLL bypass mode. HIGH = All outputs PLL bypass OPEN = C output bank PLL bypass LOW = All outputs PLL enabled
S3	DM	Selects input divider M. See Table 2.
S5	DP	Selects VCO prescale divider P. See Table 2.
S6, S7	DF1, DF0	Selects feedback divider F. See Table 2.
S8, S9	DA1, DA0	Selects output divider A. See Table 2.
S10, S11	DB1, DB0	Selects output divider B. See Table 2.
S12, S13	DC1, DC0	Selects output divider C. See Table 2.
S14	QA_CTRL1	Selects QA[2:0] output interface (LVPECL, LVDS, or DISABLED).
S15	QA_CTRL2	Selects QA[4:3] output interface (LVPECL, LVDS, or DISABLED).
S16	QB_CTRL	Selects QB[2:0] output interface (LVPECL, LVDS, or DISABLED).
S17	QC_CTRL	Selects QC and QCC output interface. LVPECL = QC output LVPECL, QCC output LVC MOS DISABLED = QC and QCC disabled LVDS = QC output LVDS, QCC output LVC MOS
S18	QA_TERM1	Selects QA[2:0] output termination. Provides DC path to GND for QA[2:0] bias-Ts when switched to LVPECL. DC path to GND is open when switched to LVDS.
S19	QA_TERM2	Selects QA[4:3] output termination. Provides DC path to GND for QA[4:3] bias-Ts when switched to LVPECL. DC path to GND is open when switched to LVDS.
S20	QB_TERM	Selects QB[2:0] output termination. Provides DC path to GND for QB[2:0] bias-Ts when switched to LVPECL. DC path to GND is open when switched to LVDS.
S21	QC_TERM	Selects QC output termination. Provides DC path to GND for QC bias-Ts when switched to LVPECL. DC path to GND is open when switched to LVDS.

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Table 2. Divider Settings for Various Frequency Configurations

INPUT FREQUENCY (MHz)	INPUT DIVIDER	FEEDBACK DIVIDER		VCO FREQUENCY (MHz)	PRESCALE DIVIDER	OUTPUT DIVIDER		OUTPUT* FREQUENCY (MHz)	APPLICATIONS		
	DM	DF1	DF0		DP	DA1 DB1 DC1	DA0 DB0 DC0				
30.72	LOW	HIGH	HIGH	3932.16	LOW	LOW	LOW	491.52	Wireless Base Station: WCDMA, cdma2000®, LTE, TD_SCDMA		
61.44	HIGH	HIGH	HIGH			HIGH	LOW	245.76			
122.88	OPEN	HIGH	HIGH			OPEN	HIGH	122.88			
33.3	LOW	HIGH	OPEN	4000	HIGH	LOW	LOW	400	Server, FB-DIMM, Network Processor, DDR/ QDR Memory, PCIe®, SATA		
66.7	HIGH	HIGH	OPEN			LOW	HIGH	266.67			
133.3	OPEN	HIGH	OPEN			HIGH	LOW	200			
25	LOW	HIGH	HIGH			HIGH	OPEN	133.333			
50	HIGH	HIGH	HIGH			OPEN	HIGH	100			
100	OPEN	HIGH	HIGH			OPEN	LOW	66.67			
33.3	LOW	OPEN	HIGH			4000	LOW	LOW		LOW	500
66.7	HIGH	OPEN	HIGH					LOW		HIGH	333.33
133.3	OPEN	OPEN	HIGH	HIGH	LOW			250			
25	LOW	LOW	OPEN	HIGH	HIGH			200			
50	HIGH	LOW	OPEN	HIGH	OPEN			166.67			
100	OPEN	LOW	OPEN	OPEN	HIGH			125			
31.25	LOW	HIGH	HIGH	LOW	OPEN			100			
62.5	HIGH	HIGH	HIGH	OPEN	OPEN			66.67			
125	OPEN	HIGH	HIGH	LOW	OPEN			50**			
				OPEN	LOW			33.33**			
32.76	LOW	HIGH	OPEN	3931.2	HIGH	HIGH	OPEN	131.04	Microwave Radio Link		
						OPEN	LOW	65.52			
20.82857	LOW	HIGH	HIGH	3999.084	OPEN	LOW	LOW	333.257	OTU1, 10Gbps SONET with FEC		
41.6571	LOW	HIGH	LOW			HIGH	LOW	166.6285			
25.78125	LOW	LOW	LOW	3867.1875	OPEN	HIGH	LOW	161.1328125	10Gbps Ethernet with FEC		
27.392578	LOW	HIGH	OPEN	3944.531232	OPEN	HIGH	LOW	164.355468	10Gbps FC		
20.916	LOW	HIGH	HIGH	4015.95949	OPEN	LOW	LOW	334.66	OTU2, 10Gbps SONET with Digital Wrapper		
41.8329	LOW	HIGH	LOW			HIGH	LOW	167.33			

*All output divider settings applicable only for A and B output banks, unless otherwise noted.

**Output divider settings applicable only for C output bank.

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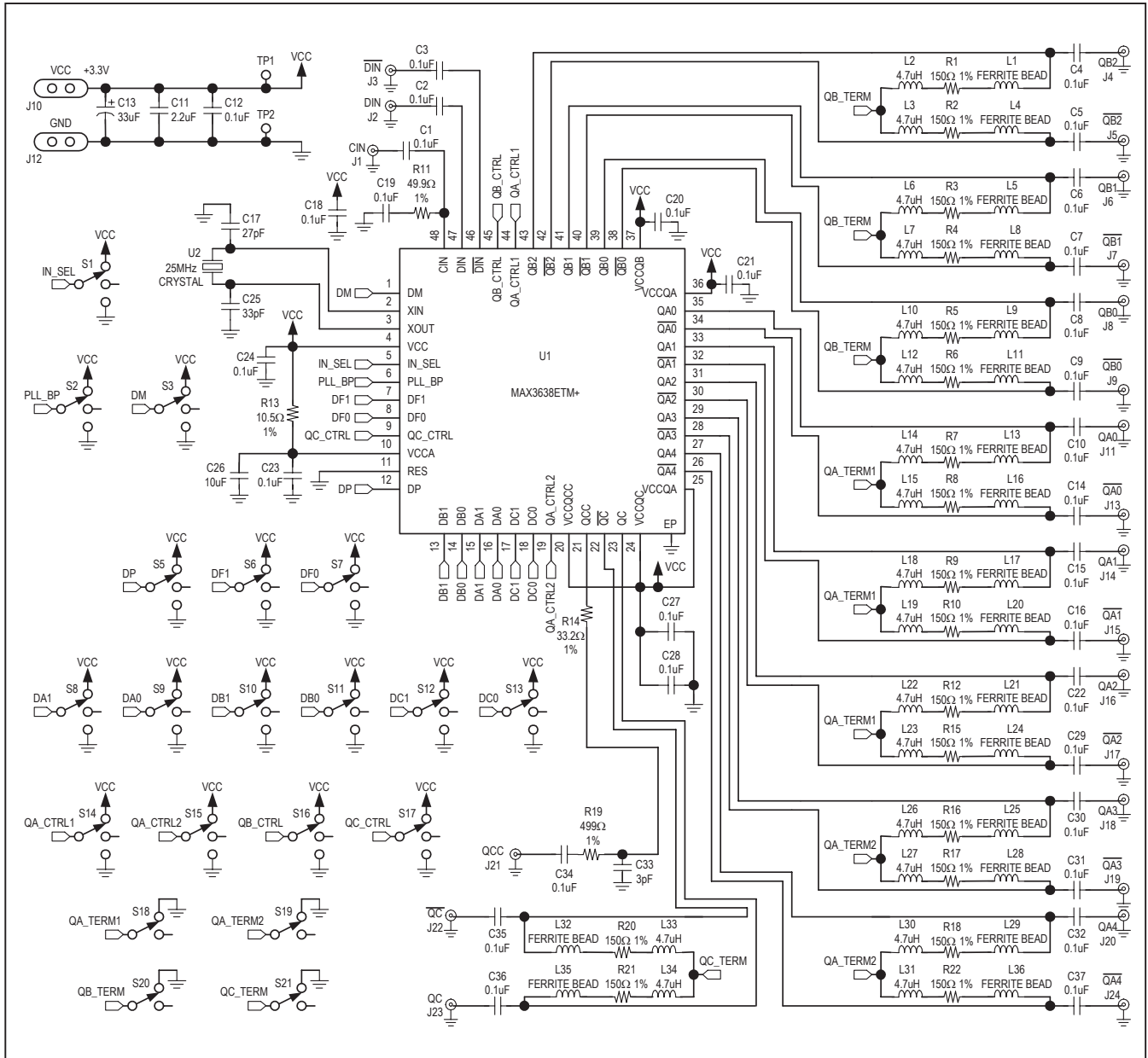


Figure 2. MAX3638 EV Kit Schematic

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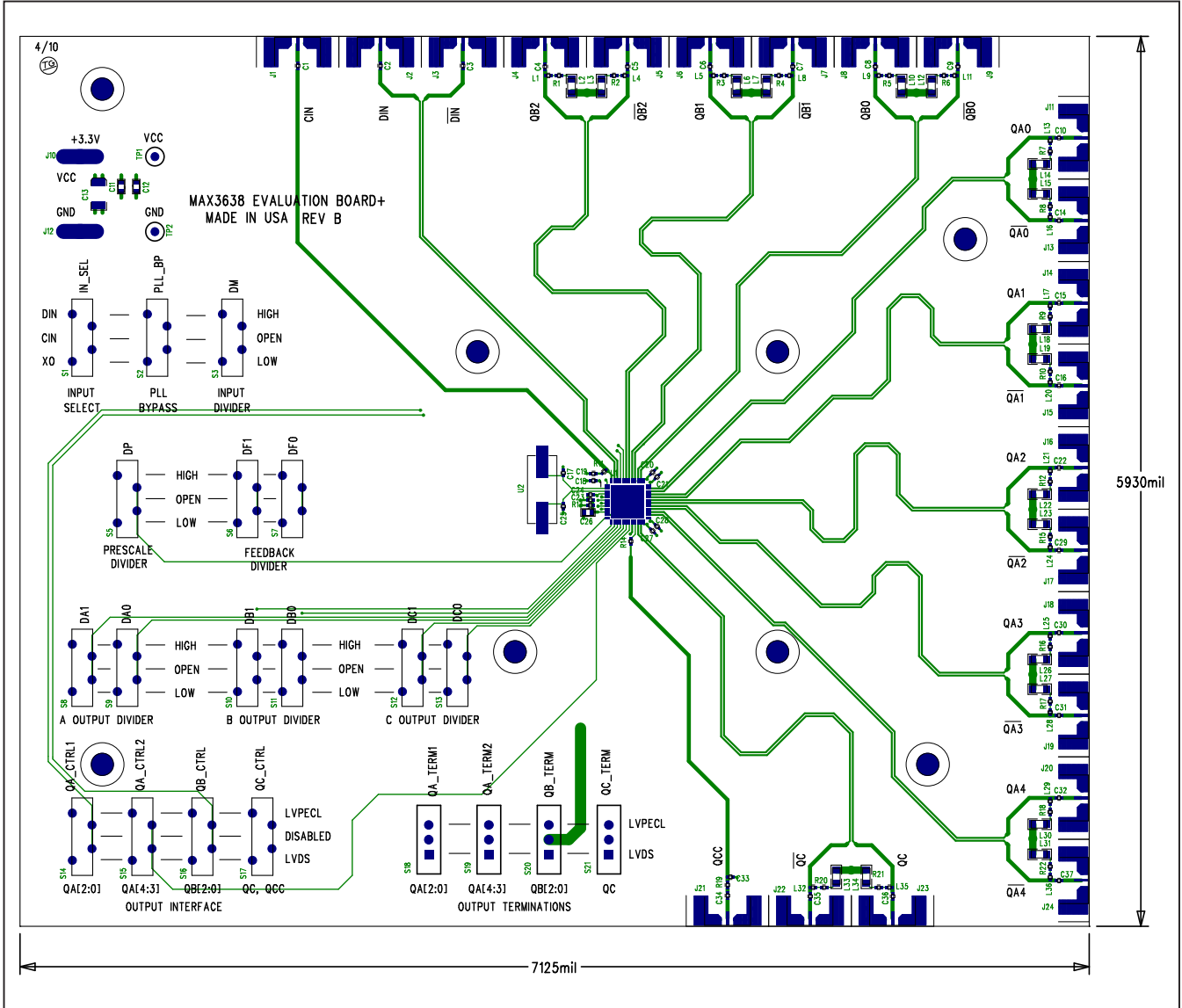


Figure 3. MAX3638 EV Kit Component Placement Guide—Component Side

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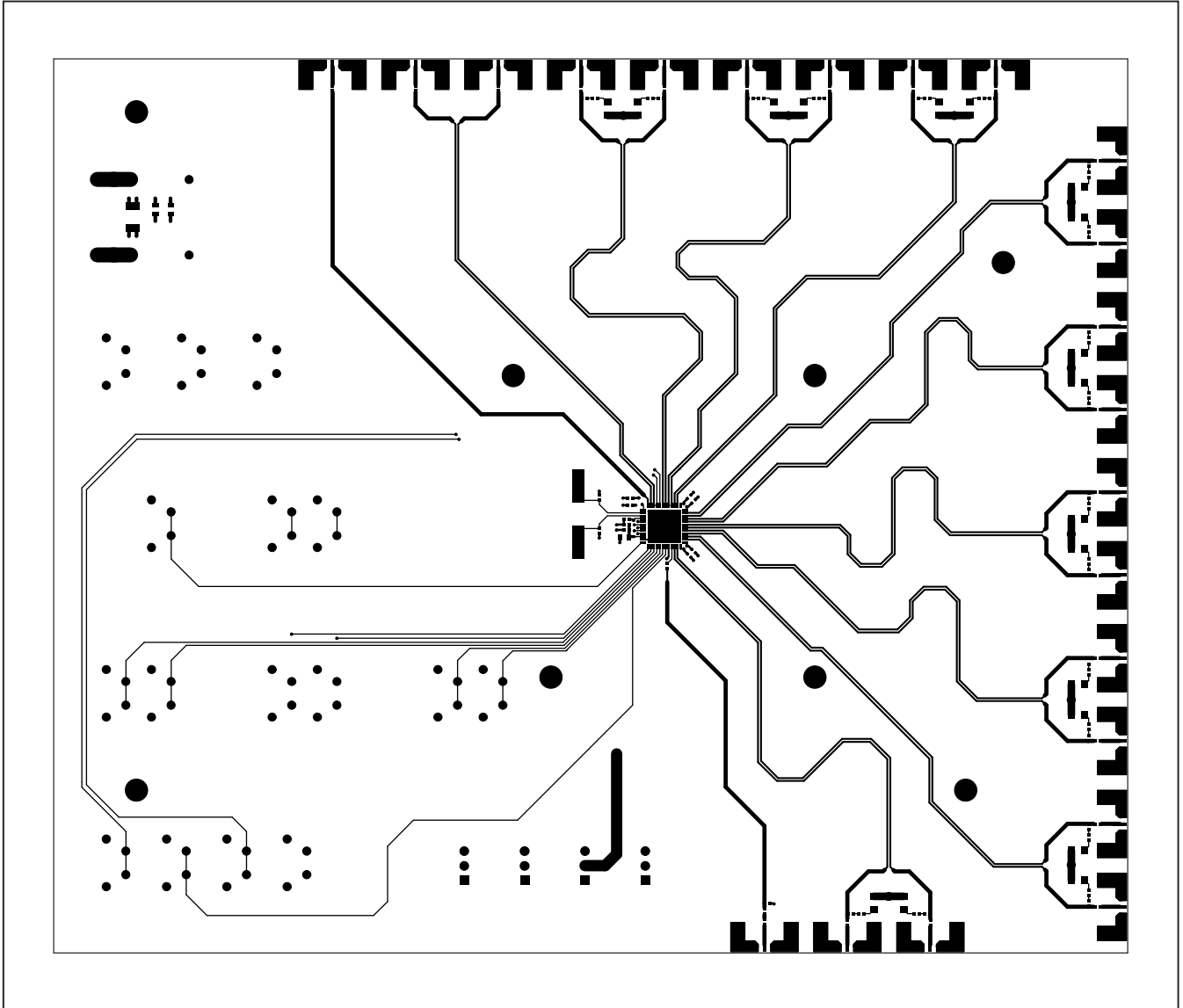


Figure 4. MAX3638 EV Kit PCB Layout—Component Side

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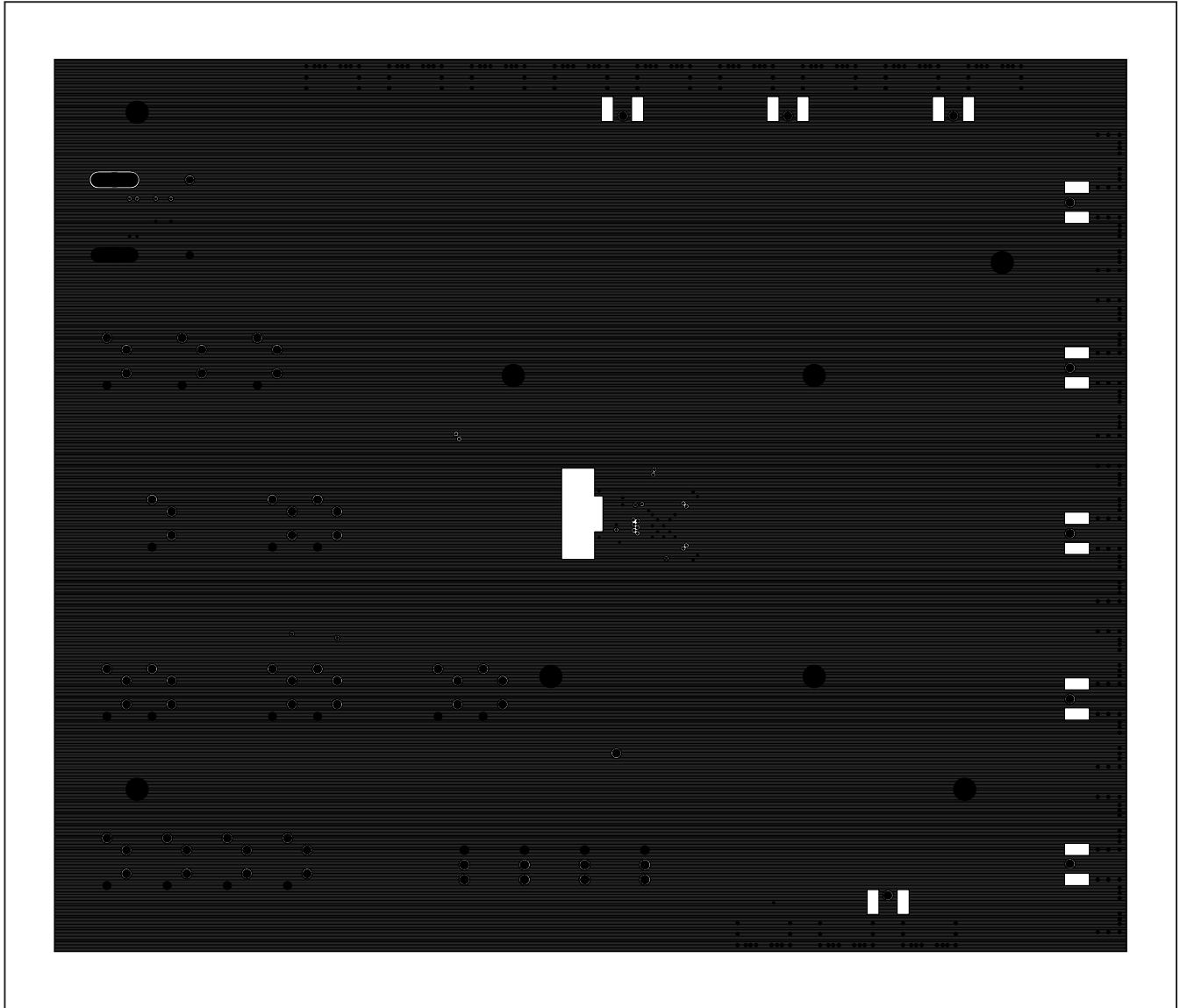


Figure 5. MAX3638 EV Kit PCB Layout—Ground Plane

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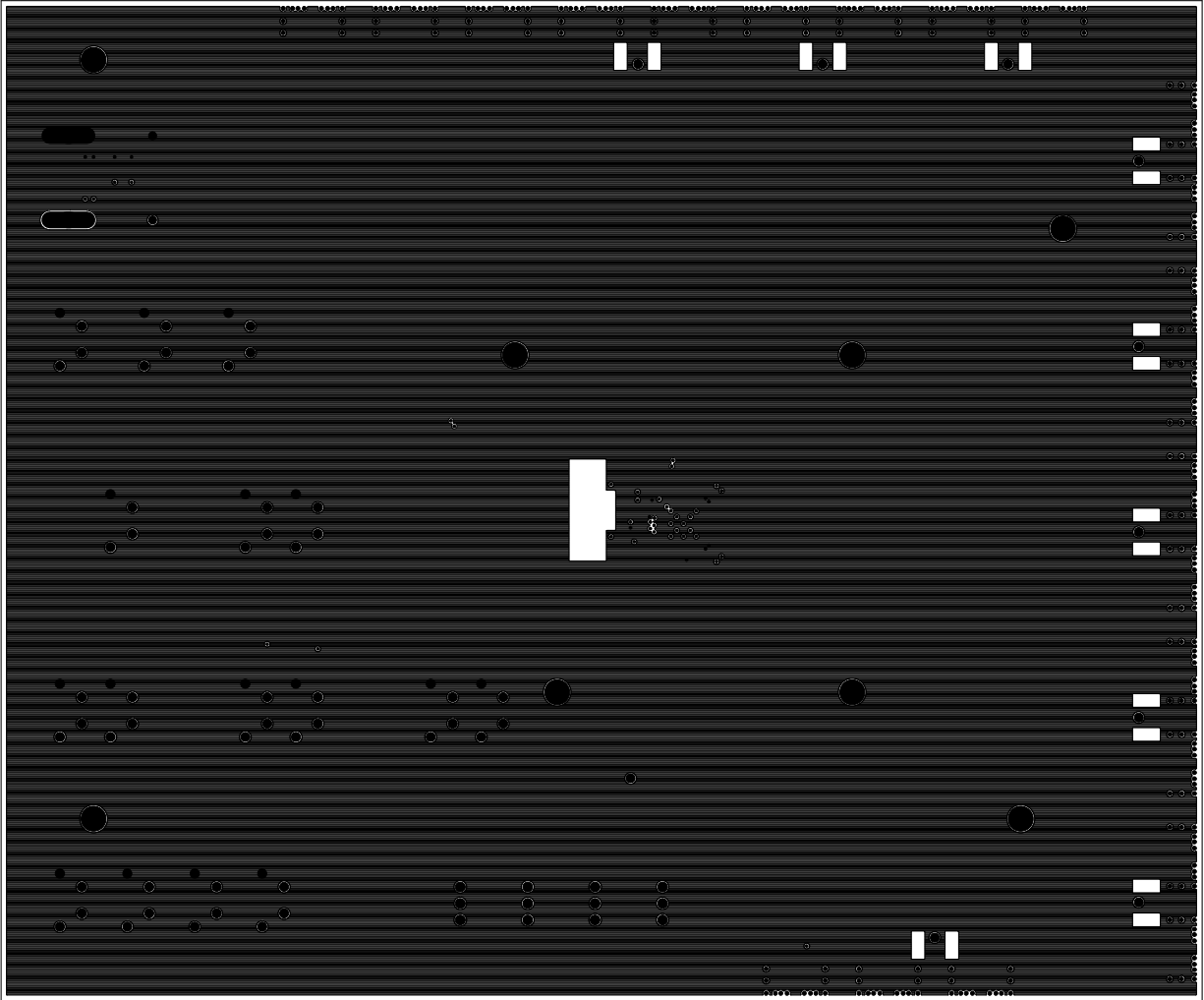


Figure 6. MAX3638 EV Kit PCB Layout—Power Plane

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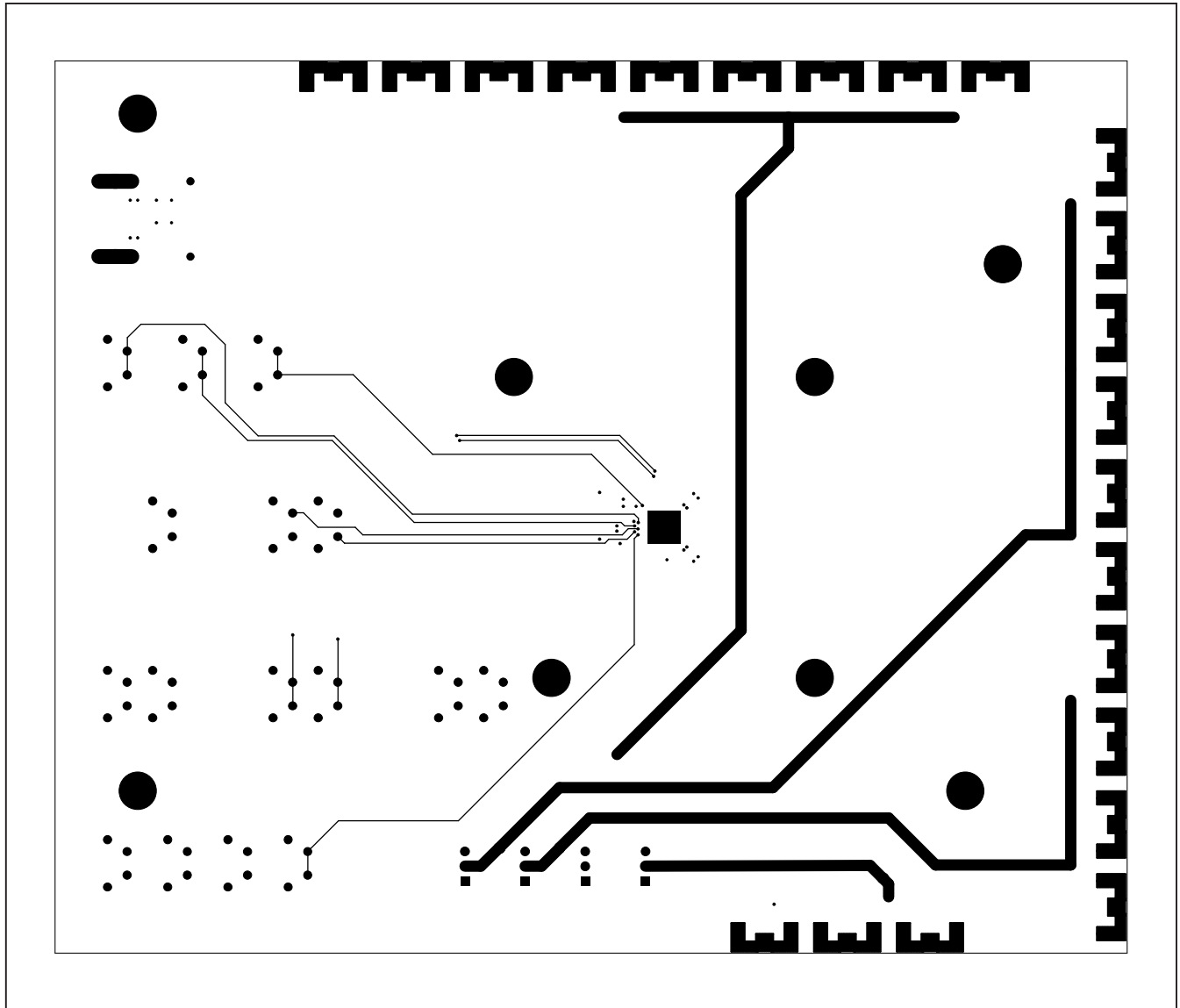


Figure 7. MAX3638 EV Kit PCB Layout—Solder Side

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Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	5/10	Initial release	—
1	5/10	Changed R13 from 10.0 Ω to 10.5 Ω in the <i>Component List</i> and Figure 2; corrected the label for L28 in Figure 2	1, 5

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